Application No.: 10/605,699 Attorney Docket No.: 21806-00156-US

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application:

LISTING OF CLAIMS:

1. (Previously presented) A CMOS semiconductor structure comprising:

a substrate;

a plurality of circuit structures formed upon said substrate, wherein at least one of said circuit structures has a susceptibility to a latch-up condition;

an injection site associated with said CMOS semiconductor structure; and

a plurality of contact regions inter-spaced a varying distance between said circuit structures.

2. (Original) The semiconductor structure of claim 1, wherein said distance varies with the proximity of said contact regions to said injection site.

3. (Original) The semiconductor structure of claim 1, wherein said distance varies with the susceptibility of said circuit structures to a latch-up condition.

4. (Original) The semiconductor structure of claim 1, wherein said plurality of contact regions comprises a first contact region and a second contact region spaced a first distance apart, and said second contact region and a third contact region spaced a second distance apart different from said first distance.

5. (Original) The semiconductor structure of claim 4, wherein said first distance is greater than said second distance.

6. (Original) The semiconductor structure of claim 4, wherein said first distance is less than said second distance.

7. (Original) The semiconductor structure of claim 1, wherein said substrate comprises a well region having formed therein said latch-up susceptible circuit structure.

8. (Original) The semiconductor structure of claim 7, wherein said well region is n-type.

9. (Original) The semiconductor structure of claim 8, wherein said n-type well region includes at least one contact comprising an n+ region.

10. (Original) The semiconductor structure of claim 9, wherein said at least one contact is coupled to Vdd.

11. (Original) The semiconductor structure of claim 7, wherein said well region is p-type.

12. (Original) The semiconductor structure of claim 11, wherein said p-type well region includes at least one contact comprising a p+ region.

13. (Original) The semiconductor structure of claim 12, wherein said at least one contact is coupled to ground.

14. (Original) The semiconductor structure of claim 12, wherein said at least one contact is coupled to Vss.

15. (Original) The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged vertically relative to said axis.

16. (Original) The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged horizontally relative to said axis.

17. (Original) The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis and arranged concentrically relative to said axis.

18. (Original) The semiconductor structure of claim 1, wherein said distance is determined such that said latch-up susceptible circuit structure is prevented from latching-up when carriers are injected into the substrate from an external current injector.

19. (Original) The semiconductor structure of claim 18, wherein said external current injector is a cable discharge arising from a cable discharge event.

20. (Original) The semiconductor structure of claim 1, wherein said distance increases as the distance of said plurality of contact regions from said injection site increases.

21. (Original) The semiconductor structure of claim 1, wherein said plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from said injection site increases.

22. (Previously presented) A method of forming a CMOS semiconductor structure having improved latch-up robustness, the method comprising the steps of:

providing a substrate including an injection site associated with said CMOS semiconductor structure and a plurality of circuit structures, wherein at least one of said circuit structures has a susceptibility to a latch-up condition; and

forming a plurality of contact regions inter-spaced a varying distance between said circuit structures.

23. (Original) The method of claim 22, wherein said distance varies with the proximity of said plurality of contact regions to said injection site.

24. (Original) The method of claim 22, wherein said distance varies with the susceptibility of said circuit structures to a latch-up condition.

25. (Original) The method of claim 22, wherein said step of forming comprises forming a first contact region and a second contact region spaced a first distance apart, and said second contact region and a third contact region spaced a second distance apart different from said first distance.

26. (Original) The method of claim 25, wherein said first distance is greater than said second distance.

27. (Original) The method of claim 25, wherein said first distance is less than said second distance.

28. (Original) The method of claim 22, wherein said distance is determined such that said latch-up susceptible circuit structure is prevented from latching-up when carriers are injected into the substrate from an external current injector.

29. (Original) The method of claim 28, wherein said external current injector is a cable discharge arising from a cable discharge event.

30. (Original) The method of claim 22, wherein said distance increases as the distance of said plurality of contact regions from said injection site increases.

31. (Original) The method of claim 22, wherein said plurality of contact regions are located along an axis so that spacing between adjacent contact regions increases as the distance from said injection site increases.

32. (Withdrawn) A program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform a method of designing an integrated circuit, the method comprising the steps of: receiving an integrated circuit design, said design providing for a plurality of circuit structures within a substrate; identifying at least one injection site associated with said integrated circuit design; identifying circuit structures as susceptible to a latch-up condition; determining a plurality of contacts for said circuit structures susceptible to a latch-up condition, said quantity being that necessary to suppress a latch-up condition within said identified circuit structures; and determining a location for said contacts so that said contacts are located to have a distance that varies with the proximity of said contacts to said at least one injection site.

33. (Withdrawn) The method of claim 32, wherein said substrate comprises a well region having formed therein at least one of said latch-up susceptible circuit structures.

34. (Withdrawn) The method of claim 32 further comprising the step of determining an aggregate contact layout.

35. (Withdrawn) The method of claim 32, wherein the step of determining said distance comprises limiting said quantify of contacts to a minimum number that suppresses a latch-up condition within said latch-up susceptible circuit structures.

36. (Withdrawn) The method of claim 32, wherein the step of determining said distance comprises identifying an aggregate contact layout responsive to said distance determination.

37. (Withdrawn) The method of claim 32, wherein the step of identifying said at least one injection site comprises identifying a location and an injection current magnitude for said at least one injection site.

38. (Withdrawn) The method of claim 32, wherein the step of identifying circuit structures as susceptible to a latch-up condition comprises identifying a location and physical attributes for each of said circuit structures susceptible to a latch-up condition.

39. (Withdrawn) The method of claim 38, wherein one of said physical attributes is resistance.

40. (Withdrawn) A computer-readable medium having a plurality of computer executable instructions for causing a computer to design an integrated circuit, the computer executable instructions comprising the steps of: receiving an integrated circuit design, said design providing for a plurality of circuit structures within a substrate; identifying at least one injection site associated with said integrated circuit design; identifying circuit structures as susceptible to a latch-up condition; determining a quantity of contacts for said circuit structures susceptible to a latch-up condition, said quantity being that necessary to suppress a latch-up condition within said identified circuit structures; and determining a varying distance for said contacts, wherein said distance varies with the proximity of said contacts to said at least one injection site.

41. (Withdrawn) The computer-readable medium of claim 40, wherein said medium comprises hardware.

42. (Withdrawn) The computer-readable medium of claim 40, wherein said medium comprises firmware.

43. (Withdrawn) The computer-readable medium of claim 40, wherein said computer-readable medium is configured to maintain one or more data structures and store data, wherein said instructions are executed seriatim as part of a loop structure wherein retrieved data is stored within said one or more data structures.

44. (Withdrawn) The computer-readable medium of claim 43, wherein said data originates externally from the medium.

45. (Withdrawn) The computer-readable medium of claim 40, wherein said instructions are executed to retrieve data from one or more data structures, said data representing variables associated with said substrate, circuit structures, wells, contacts, and periodicity.

46. (Withdrawn) The computer-readable medium of claim 40, wherein said design is software implemented and comprises software components that represent constituent elements of the design.

47. (Withdrawn) The computer-readable medium of claim 46, wherein said constituent elements include substrate, circuit structures, and wells.

48. (Withdrawn) The computer-readable medium of claim 46, wherein said software components comprise data structures.

49. (Withdrawn) The computer-readable medium of claim 48, wherein said data structures are embedded within said software implemented design.

50. (Withdrawn) The computer-readable medium of claim 46, wherein said software components maintain data and wherein said instructions are executed to retrieve data from said software components, said data representing variables associated with said substrate, circuit structures, wells, contacts, and periodicity.

51. (Withdrawn) The computer-readable medium of claim 48, wherein said design is implemented in an object oriented platform and said data structures are objects.